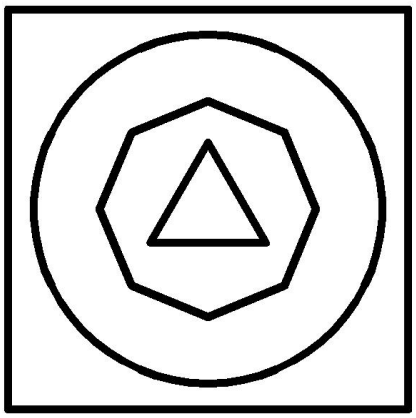
4-1 选择器



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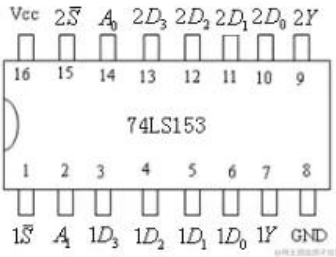
1、双4选1数据选择器74LS153

所谓双4选1数据选择器，就是在一块集成芯片上集成两个完全独立的4 选1 数据选择器，其引脚排列如图2所示，功能如表1所示。



输　入			输　出
$\overline{S}$	A_1	A_0	Y
1	×	×	0
0	0	0	D_0
0	0	1	D_1
0	1	0	D_2
0	1	1	D_3

复制代码

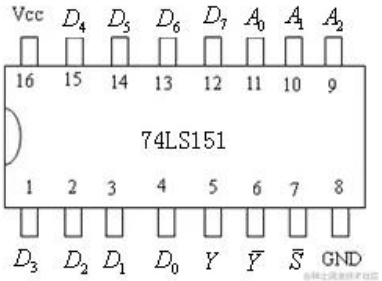
1　图2双4选1数据选择器74LS153引脚排列图　　表1 数据选择器74LS153功能表

4选1数据选择器的逻辑表达式可写为

$$Y=(\overline{A}_1\overline{A}_0D_0+\overline{A}_1A_0D_1+A_1\overline{A}_0D_2+A_1A_0D_3)S$$

2、8选1数据选择器74LS151

74LS151为互补输出的8选1数据选择器，其引脚排列如图3所示，功能如表2所示。



输　入				输　出
$\overline{S}$	A_2	A_1	A_0	Y
1	×	×	×	0
0	0	0	0	D_0
0	0	0	1	D_1
0	0	1	0	D_2
0	0	1	1	D_3
0	1	0	0	D_4
0	1	0	1	D_5
0	1	1	0	D_6
0	1	1	1	D_7

8-to-1 Multiplexer

An 8-to-1 multiplexer consists of eight data inputs D0 through D7, three input select lines S0 through S2 and a single output line Y. Depending on the select lines combinations, multiplexer selects the inputs.

The below figure shows the block diagram of an 8-to-1 multiplexer with enable input that can enable or disable the multiplexer. Since the number data bits given to the MUX are eight, then 3 bits (23 = 8) are needed to select one of the eight data bits.

Block Diagram of 8-to-1 Multiplexer

The truth table for an 8-to1 multiplexer is given below with eight combinations of inputs so as to generate each output corresponds to input.

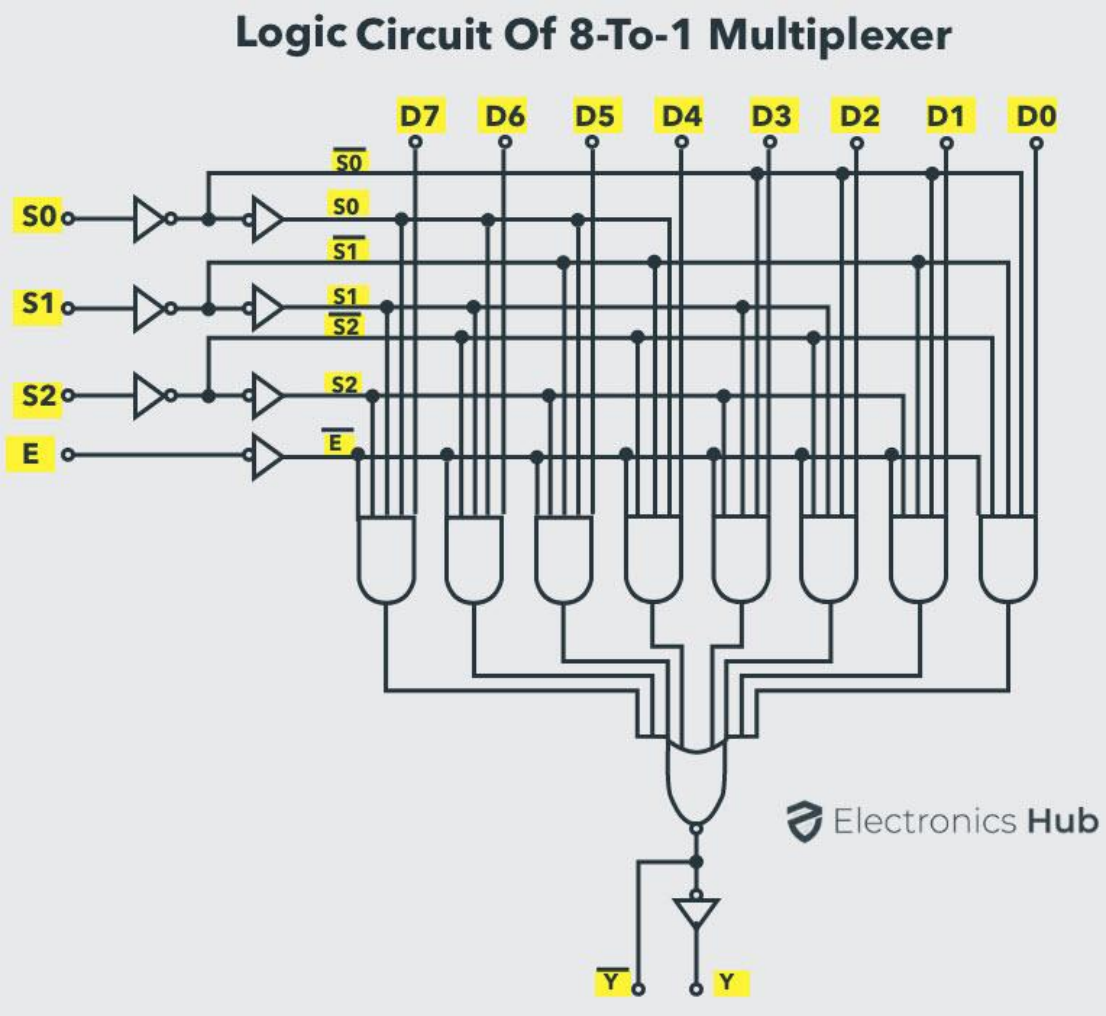
For example, if S2= 0, S1=1 and S0=0 then the data output Y is equal to D2. Similarly the data outputs D0 to D7 will be selected through the combinations of S2, S1 and S0 as shown in below figure.

S0	S1	S2	D0	D1	D2	D3	D4	D5	D6	D7	Y
0	0	0	0	X	X	X	X	X	X	X	0
0	0	0	1	X	X	X	X	X	X	X	1
0	0	1	X	0	X	X	X	X	X	X	0
0	0	1	X	1	X	X	X	X	X	X	1
0	1	0	X	X	0	X	X	X	X	X	0
0	1	0	X	X	1	X	X	X	X	X	1
0	1	1	X	X	X	0	X	X	X	X	0
0	1	1	X	X	X	1	X	X	X	X	1
1	0	0	X	X	X	X	0	X	X	X	0
1	0	0	X	X	X	X	1	X	X	X	1
1	0	1	X	X	X	X	X	0	X	X	0
1	0	1	X	X	X	X	X	1	X	X	1
1	1	0	X	X	X	X	X	X	0	X	0
1	1	0	X	X	X	X	X	X	1	X	1
1	1	1	X	X	X	X	X	X	X	0	0
1	1	1	X	X	X	X	X	X	X	1	1

From the above truth table, the Boolean equation for the output is given as:

$$Y = S0\ S1\ S2\ D0 + S0\ S1\ S2\ D1 + S0\ S1\ S2\ D2 + S0\ S1\ S2\ D3 + S0\ S1\ S2\ D4 + S0\ S1\ S2\ D5 + S0\ S1\ S2\ D6 + S0\ S1\ S2\ D7$$

From the above Boolean equation, the logic circuit diagram of an 8-to-1 multiplexer can be implemented by using 8 AND gates, 1 OR gate and 7 NOT gates as shown in below figure. In the circuit, when enable pin is set to one, the multiplexer will be disabled and if it is zero, then select lines will select the corresponding data input to pass through the output.



Logic Circuit of 8-to-1 MUX

IC 74151 is a popular 8-to-1 multiplexer IC with eight inputs and two outputs. The two outputs are active low and active high outputs. It has three select lines A, B and C and one active low enable input. The pinout of this IC is given below.